St. Thomas' College of Engineering and Technology

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Newsletter

Department

ECE

DARPAN

(The Image of Achievements)

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Vision of ECE Department:

To build a strong teaching and research environment to cater to the manpower needs in Industrial and Academic domains of the rapidly growing Electronics and Communication Engineering.

Mission of ECE Department:

- To produce certified industry-ready professional in Electronics and Communication Engineering, though innovative educational programs incorporating laboratory practices and project based teaching-learning processes, in a modern environment.

- To create knowledge base of advanced technologies through research in the area of Electronics and Communication, for competitive and sustainable development of the country.

- To groom the department as a learning centre to inculcate advancement of technology in Electronics and Communication Engineering with social values and environmental awareness.

Recent Technology Trend

In the last three decades the Integrated Circuits (ICs) follow a steady path toward shrinking the device dimensions without affecting the functionality of the chips. The scaling down of the device dimensions leads to secondary effects, such as sub-threshold leakage, gate leakage, DIBL etc. Structural modifications need to be incorporated in order to avoid the short channel effects. Amongst those modifications, double gate, high mobility channel, surrounded gate and FinFETs are the promising candidates. Needs of low power devices for improving battery life and device reliability are increasing day by day. Power management approach needs to be adopted which includes dynamic power minimization approach, leakage power minimization approach etc. Hence, it is a big challenge for the designer to design a sustainable low power device. On the other hand, advancement of the process technology in deep sub-micron (DSM) region leads to gate delays to be comparable with the wire delays. Technology scaling also enables hundreds of processing elements (PEs) to be integrated on a single chip. As a result, efficient placement of the PEs on a chip floor plan along with a scalable communication infrastructure design plays a crucial role in determining the system performance as well as the system reliability.

Dr. Prasun Chowdhury
Head of the Department,
Department of Electronics and Communication Engineering

Departmental Milestones

Best Performance in MAKAUT:

- Roshon Kumar Jha, 4th Year, 8th Semester, SGPA: 9.46
- Debomita Chakraborty, 3rd Year, 6th Semester, SGPA : 9.56
- Swapnanil Gupta, 2nd Year, 4th Semester, SGPA: 9.65

Performance in Competition:

- Sanjana Ghoshal, 1st Year, received 1st position in All India Essay Competition organized by Shri Ram Chandra Mission (SRCM) & United Nations Information Centre for India & Bhutan (UNIC)

- Abriti Guha, 2nd Year ECE, received 2nd position for INNOVATION in SREY 2017, organized by Students of STCET.

Faculty Development Programme

- **Mrs. Kakali Das** and Ms. Tanusree Dutta attended the Short Term Training Programme on SCILAB, held at National Institute of Technical Teachers Training and Research (NITTTR), Kolkata from 19th June to 30th June, 2017 (2 Weeks).

- **Mr. Prashnatita Pal** attended a training program on "Art of Microcontroller", which was held at Indian institute of Technology, Kharagpur from 19th June to 30th June, 2017 (2 Weeks) .

Event organized

Name of event: Workshop on "Basics of Embedded systems"

Date: 20th to 22nd June, 2017

This workshop was conducted to gather knowledge about embedded systems through lectures given by two eminent professors from IITKGP: Dr**.** Santanu Chottapadhyay on "Embedded Systems- An Overview" and by Dr. Indranil Sengupta on "Security in Embedded Systems".

Based on the performance in quiz as well as hands-on session, out of sixty eight participants three students, Kaustav Bandyopadhyay, Kaustav Sarkar and Subhadip Ghosh were awarded 1st, 2nd and 3rd Position respectively.

Publication Details

1. Souvik De, Sneh Agarwal, **Dr. Prasun Chowdhury** and **Supriyo Sengupta,** "Payroll Management System with Biometric ID", Proceedings of IEEE, ICTPACT, Apr., 2017, Chennai.

2**. A. Chattopadhyay**, R. Das, A. Dasgupta, A. Kundu, Chandan K. Sarkar, "A linearity based comparison between symmetric and asymmetric lateral diffusion for a 22 nm Underlapped DG-MOSFET", Superlattices and Microstructures, pp 69-82, Apr. 2017.

3**. A. Chattopadhyay**, A. Dutta, A. Kundu, Chandan K. Sarkar, "Effect of Channel Engineering on Analog/RF Performance of Underlapped Gatestack DG-MOSFET in Sub-20nm Regime", Devices for Integrated Circuit (DevIC) 2017.

4. Sachin Seth, Sudipto Mukherjee, **Tanusree Dutta** and **Rabindranath Ghosh,** " Storage Efficiency Optimization of a Super Capacitor charged by a Photovoltaic Cell using Genetic Algorithm", International Advanced Research Journal in Science, Engineering and Technology, Vol. 4, Issue 5, May 2017.